Pluto 5 Calypso 16 Card Manual

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1 INTRODUCTION

The Pluto 5 Calypso 16 card provides a high performance video capability for the Pluto 5 family of products. The card represents an evolutionary development of the CGA/VGA video system. It provides enhanced performance while maintaining compatibility with software written for the Pluto 5 video system.

The card additionally provides:

- A standard IDE interface, to which a Hard Drive or ATAPI CD-ROM can be connected.
- An RS232 serial port, which can be used to connect to a touch screen.
- Expansion EPROM.

This manual covers the detail of the hardware operation of the Pluto 5 CGA/VGA Card.
The Software Driver functions that provide the Application Interface to this board are described
In a separate document, the Pluto 5 Software User Manual, Heber Document number 80-16040

2 OVERVIEW

The Pluto 5 CALYPSO 16 Card is an add-on board for the Pluto 5 Controller Board, which plugs into the Memory and I/O Expansion Card Connectors. The Memory Expansion Card Connector is duplicated on the CALYPSO 16 Card, allowing a Pluto 5 Memory Expansion Card to also be fitted.

The card is based around a Fujitsu Cremson Graphics Controller IC, and will directly drive an analogue colour monitor. This device supports a number of screen resolutions varying from CGA (640x225) to SVGA (1024 x 768).

Supported colour depths are 8 bits per pixel (256 colours) and 16 bits per pixel (32, 768 colours).

Calypso 16 is fitted with 16 Mbyte of Video Display Memory. In addition, two 42 pin EPROM sockets are provided, allowing up to 8 Mbytes of expansion EPROM to be fitted.

A standard 40 pin IDE connector is fitted, which provides an interface to a Hard Drive or CD-ROM.

3 CIRCUIT SCHEMATIC DESCRIPTION

This section is a walk through of the Pluto 5 CALYPSO 16 Card circuit schematics, document number 56-16318. A detailed description is given in Section 4 "CIRCUIT OPERATION".

3.1 Sheet 1

This sheet shows the interconnection between the remaining sheets of this drawing.

3.2 Sheet 2

This sheet shows the following items: -

- Address and Data bus buffers.
- Pluto 5 I/O and Memory Expansion Connectors. (P1 and P2)
- Duplicated Memory Expansion Connector. (P3)

3.3 Sheet 3

This sheet shows the following items: -

- IDE Connector. (P4)
- Two 42 pin EPROM Expansion Sockets. (U1 and U2)
- RS232 Interface and Connector. (P5)

3.4 Sheet 4

This sheet shows the following items: -

- Xilinx FPGA.
- Serial EEPROM for initialising FPGA.

3.5 Sheet 5

This sheet shows the following items: -

- Cirrus Cremson VGA Controller.
- Video Output Connectors (P5 and P6)

3.6 Sheet 6

This sheet shows the following items: -

- Video Display Memory (16 MBytes)

3.7 Sheet 7

This sheet shows the following items: -

- Voltage Regulators.

4 CIRCUIT OPERATION

4.1 FPGA

U10 is a Xilinx XS10 FPGA (Field Programmable Gate Array). It performs the following functions: -

- Address decoding.
- Motorola CPU 32 to SH4 bus conversion
- 16 bit to 32 bit data bus translation.
- IDE Interface.
- Single channel UART
- PROM autoselect.

The Xilinx FPGA is RAM based, and the internal logic is configured during RESET by a Serial bit-stream generated by U11, which is a XC17S10XL eight pin socketed serial EEPROM

4.2 IDE Interface

The ATA-2 standard IDE interface is implemented within the FPGA, and a standard 40pin connector P4 is provided. Additional buffering is provided on the RESET line, to prevent retriggering when connected to external drives with significant capacitive loading on the RESET line.

4.3 RS232 Interface

A single UART is implemented within the FPGA. Receive RXD and transmit TXD signals are provided, together with RTS and CTS handshaking. Signal level conversion is provided by U9, a MAX232 device. The transmit clock and sixteen times receive clock are generated by subdivision from the CPU clock (16.77 MHz) giving an acceptable percentage error of 0.5 per cent.

4.4 EXPANSION CONNECTORS - BUS BUFFERING

The Pluto 5 address bus is buffered by octal buffers U4, U5, and U7. The data bus is buffered bi-directionally by U3, U8. A standard 9W D-type connector, P5, is fitted.

4.5 EPROM EXPANSION

Sockets are provided for up to two 42 pin EPROMs U1, U2. This allows up to 8Mbytes of expansion EPROM to be fitted to the board, if two 27C322 devices (2Mbyte x16) are fitted.

4.6 FUJITSU CREMSON GRAPHICS CONTROLLER

U12 is a Fujitsu Cremson device. This is configured by option links to implement a Hitachi SH4 bus interface. Bus conversion between SH4 and Motorola CPU32 type control and status signals is performed by the FPGA, together with 16 bit to 32 bit data bus conversion.

The analogue R, G, and B video outputs are terminated by R15, R16 and R17 and filtered by pi filters L7-L9, C80-85. Separate horizontal and vertical syncs are generated. Diode clamps D1, D2, D7-D9 provide protection against display monitor transients.

4.7 VIDEO DISPLAY MEMORY

A total of 16 megabytes of display memory is fitted. This uses 100MHz SDRAMs, organised as two 4M x 16 DRAMs, U14 and U15. The data path width to the Cremson controller is 32 bits. The display memory is mapped into the Pluto 5 address space via the Cremson controller.

5 OPERATION

5.1 MEMORY MAP

The default Pluto 5 system memory map is advised:

Chip Select	Function	Address	Size
CS0-	EPROM	0000 0000 - 00FF FFFF	16Mbyte
CS1-	RAM	0100 0000 - 01FF FFFF	16Mbyte
CS2-	IO/FPGA	0200 0000 - 02FF FFFF	16Mbyte
CS3-	VGA	0300 0000 - 03FF FFFF	16Mbyte

To achieve these settings, the CS registers in the SIM40 module of the 68340 should be set as follows;

SIM40 REG	VALUE	COMMENTS
I_CSAM0	00FF FFFD	All spaces, 3 wait states, 16 bit port, r only
I_CSBA0	0000 0009	0000 0000 – 00FF FFFF (EPROM, 16Mb)
I_CSAM1	000F FFFD	All spaces, 3 wait states, 16 bit port, r/w
I_CSBA1	0100 0001	0100 0000 – 010F FFFF (RAM, 16Mb)
I_CSAM2	00FF FFFF	All spaces, 3ext dtack, 16 bit port, r/w
I_CSBA2	0200 0001	0200 0000 – 02FF FFFF (PLUTO 5 FPGA, 16Mbyte)
I_CSAM3	000F FFFF	All spaces, ext dtack, 16 bit port, r/w
I_CSBA3	0300 0001	0300 0000 – 030F FFFF (VGA BOARD, 16Mb)

Note the programming of CS2 & CS3 for external DTACK operation.

5.2 CALYPSO 16 CARD MAPPING

The card is located in the memory area addressed by CS3-.

Access is mapped as 5 blocks, as follows:

FUNCTION	PLUTO 5 ADDRESS
Cremson Regs	3FC0000 – 3FFFFF
Graphics Memory	30000000 -- 3EFFFF
IDE Command Regs	3FA0000 – 3FA000F
IDE Control Regs	3FB000A
UART Control Reg	3FB0000
UART Data Reg	3FB0002

6 VIDEO CAPABILITIES

The Calypso 16 card uses the Fujitsu Cremson MB86290A graphics display controller. The Cremson graphics display controller enables an image or an animation to be displayed on the screen with display frames of up to four layers. The Cremson graphics display controller can display 8 bit and 16 bit colour

6.1 Screen Resolution

Calypso 16 works with three main screen resolutions. The screen resolutions are set in the software. The main possible screen resolutions are:

- 640 x 480
- 800 x 600
- 1024 x 768

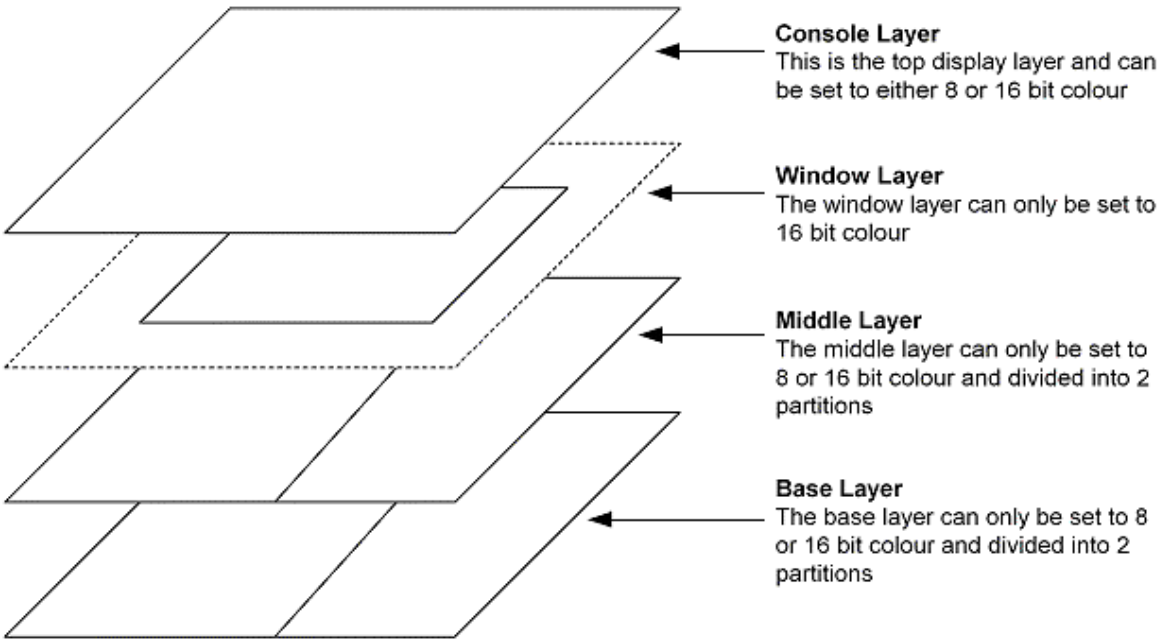
6.2 Key Features

The key features of Calypso 16 are:

- Up to 4 layers of overlaid video display frames
- 8 bit colour depth (256 colours)
- 16 bit colour depth (32, 768 colours)
- Alpha Blending (Console layer only)
- Double Buffering
- Drawing features

6.3 Video Layer Architecture

The Fujitsu Cremson video processor can display four layers of display frames on top of each other. Each layer has different display properties such as the number of bytes per pixel, the ability to be split, display priority, and possible transparency.



6.3.1 Console Layer

The Console layer contains a single logical graphics display field (**C-Layer**) which has the highest display priority and can display 8 or 16 bits per pixel images. The console layer is the only layer that allows Alpha Blending.

6.3.2 Window Layer

The Window layer contains a single logical graphics display field (**W-layer**) which has the second highest display priority and can only display 16 bits per pixel images. No transparency can be set for this layer. The window layer size (not the logical graphics field) is not necessarily full screen, unlike the other three layers. The position parameter as well as the size of the layer must be defined independently for it to be visible.

6.3.3 Middle Layer

The Middle layer is split vertically into left (**ML-Layer**) and right (**MR-Layer**) logical graphics display fields. It is possible to set one of the two to represent the dimensions of the physical display. In this case the layer behaves as though it has a single display field. The Middle left layer and Middle right layer logical graphics fields have the third highest display priority and can display 8 or 16 bits per pixel images. The Middle layer frames also support Double Buffering.

6.3.4 Base Layer

The Base layer is split vertically into left (**BL-Layer**) and right (**BR-Layer**) logical graphics display fields. It is possible to set one of them to represent the dimensions of the physical display. In this case the layer behaves as though it has a single logical graphics field. The Base left layer and Base right layer logical graphics fields have the lowest display priority and can display 8 or 16 bits per pixel images. The Base layer frames also support Double Buffering.

6.4 Performance Limitations

Calypso 16 supports 8 bit colour with up to 4 layers at all screen resolutions. Calypso 16 also supports 16 bit colour. However, at certain screen resolutions and depending on the number of layers used, there is on screen video disturbance. This is because the higher the resolution and the more layers that are used, the more data that is needed to be written to and read from memory.

6.4.1 Video Memory Bandwidth

The performance limits are fixed by the memory bandwidth between the Cremson video controller and the SDRAM video memory. On-screen disturbances occur when the required memory bandwidth is greater than the maximum memory bandwidth.

The required memory bandwidth increases with:

- screen resolution
- colour depth
- number of active display layers
- CPU to video memory activity
- Cremson drawing activity
- use of Alpha Blending

When on-screen disturbances occur, possible solutions are:

- reducing the colour resolution of the layers
- reducing the resolution of the layers
- reducing the number of layers

Heber recommends that only a certain number of layers are used at particular screen resolutions, as detailed in the table below.

6.4.2 Achievable Performance

Resolution (pixels)	8 Bit Colour				16 Bit Colour			
	1 Layer	2 Layers	3 Layers	4 Layers	1 Layer	2 Layers	3 Layers	4 Layers
640 x 480	✔	✔	✔	✔	✔	✔	✔	✔
800 x 600	✔	✔	✔	✔	✔	✔	✔	✕
1024 x 768	✔	✔	✔	✔	✔	✕	✕	✕

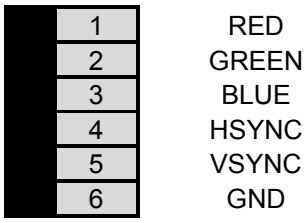
Key

✔ : OK to use these number of layers at this particular resolution
✕: Bandwidth limitation produces possible screen disturbances

7 CONNECTOR TYPES AND PIN-OUTS

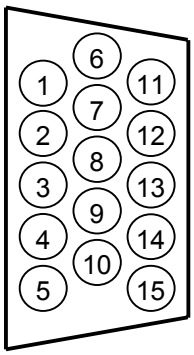
7.1 P7 - Video Output Connector

Reference: P7
Type: Header 6W AMP MTA-100
Description: Video Output Connector



7.2 P6 - Video Output Connector

Reference: P6
Type: 15W Hi-Density Dtype
Description: Video Output Connector



PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	RED	6	GND	11	nc
2	GREEN	7	GND	12	nc
3	BLUE	8	GND	13	H_SYNC
4	nc	9	nc	14	V_SYNC
5	GND	10	GND	15	nc

7.3 P3 - Memory Expansion Card Connector

Reference: P3
Type: DIN41612, C/" Socket Vertical
Description: Connector for Memory Expansion Boards

	A	*B*	*c*
1	A4	A5	A6
2	VCC	A7	A8
3	VCC	A9	A10
4	A3	A11	A12
5	A2	A13	A14
6	A1	A15	A16
7	GND	A17	A18
8	GND	A19	ROM_P1
9	MEM_BRD-	A21	D15
10	ROM_CE3-	D14	D13
11	ROM_CE4-	D12	D11
12	FPGA3	D10	D9
13	FPGA4	D8	D7
14	FPGA5	D6	D5
15	A22	D1	D3
16	D0	D2	D4

7.4 P4 - IDE Connector

Reference: P4
Type: 40W Header
Description: IDE Connector for CD-ROM

RESET-	1	2	GND
D7	3	4	D8
D6	5	6	D9
D5	7	8	D10
D4	9	10	D11
D3	11	12	D12
D2	13	14	D13
D1	15	16	D14
D0	17	18	D15
GND	19	20	KEYPIN
nc	21	22	GND
IOW-	23	24	GND
IOR-	25	26	GND
IORDY-	27	28	SYN/SEL
nc	29	30	GND
INTR	31	32	IO16-
A1	33	34	PDIAG-
A2	35	36	A3
CS1FX-	37	38	CS3FX-
DASP-	39	40	GND

Figure 1 - Calypso 16, Schematic Sheet 1

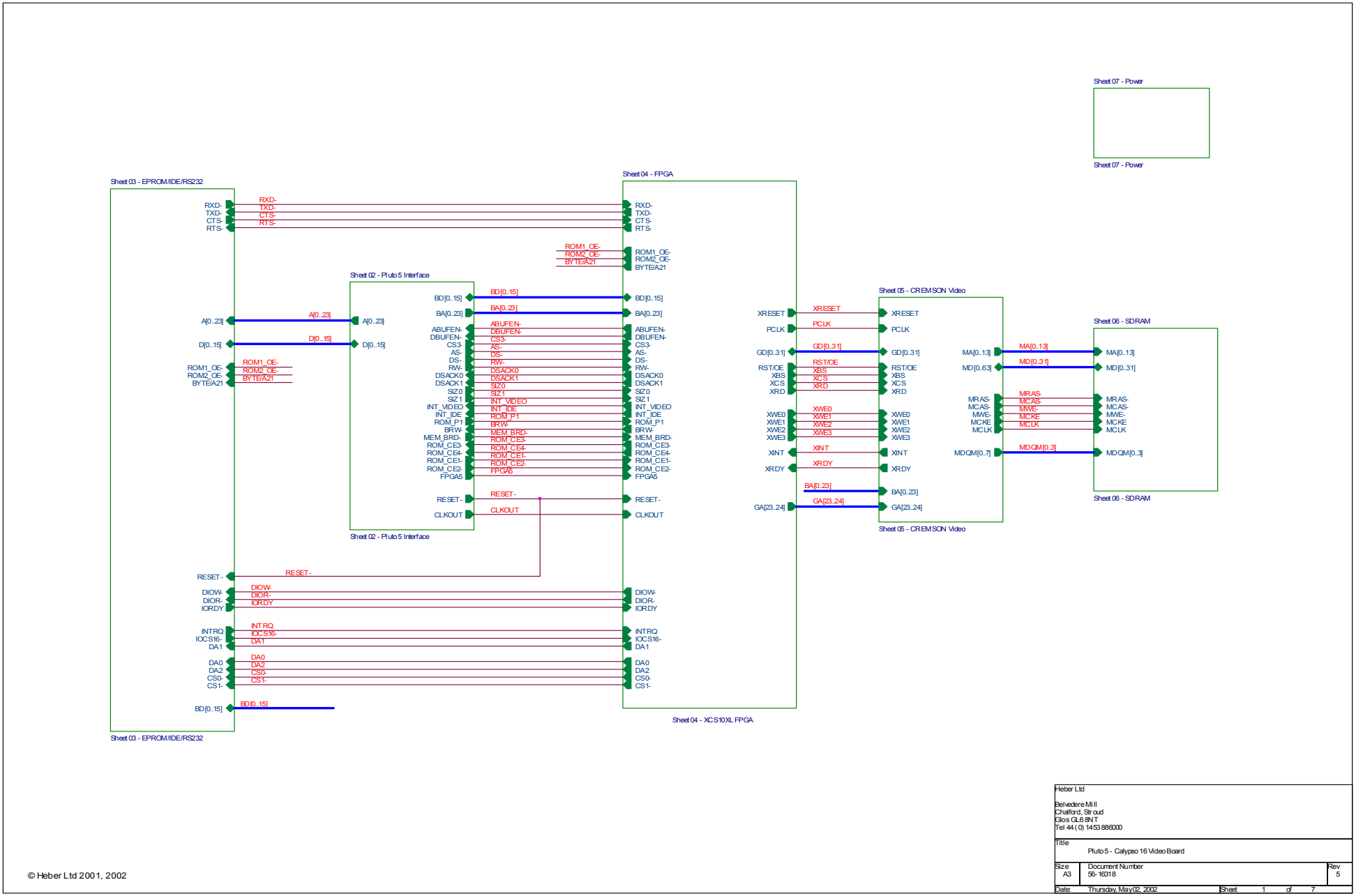


Figure 2 - Calypso 16, Schematic Sheet 2

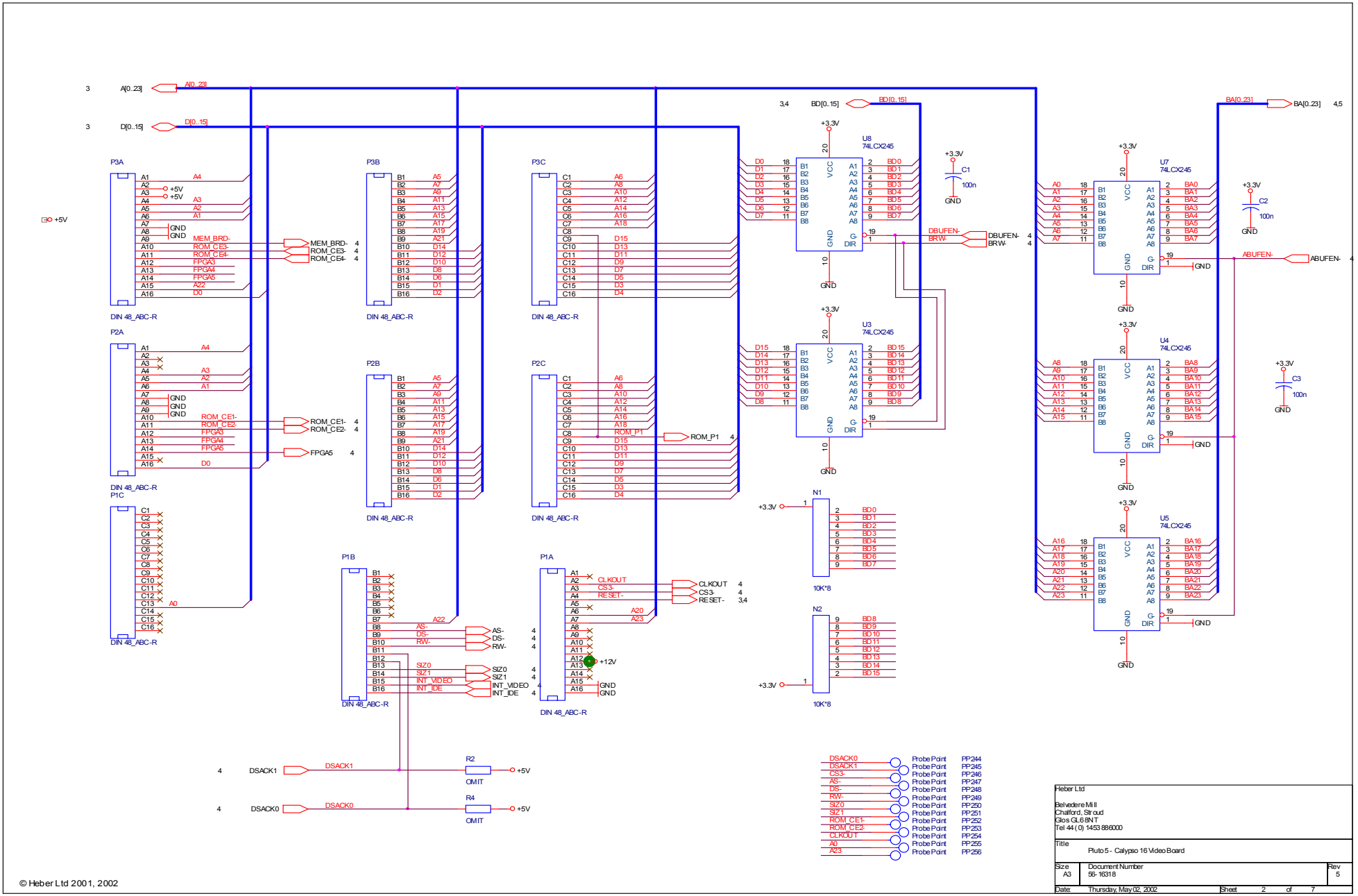


Figure 3 - Calypso 16, Schematic Sheet 3

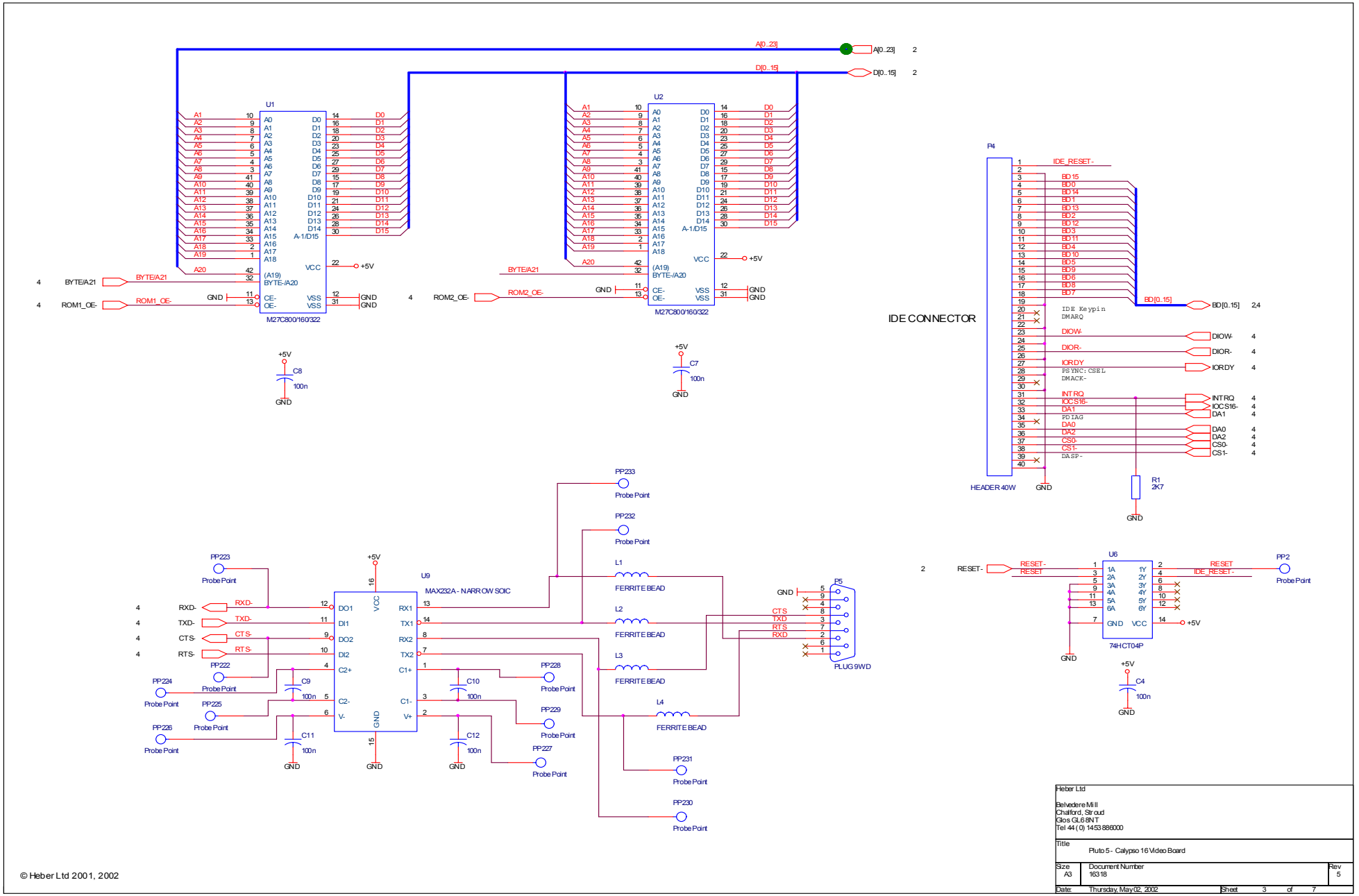


Figure 4 - Calypso 16, Schematic Sheet 4

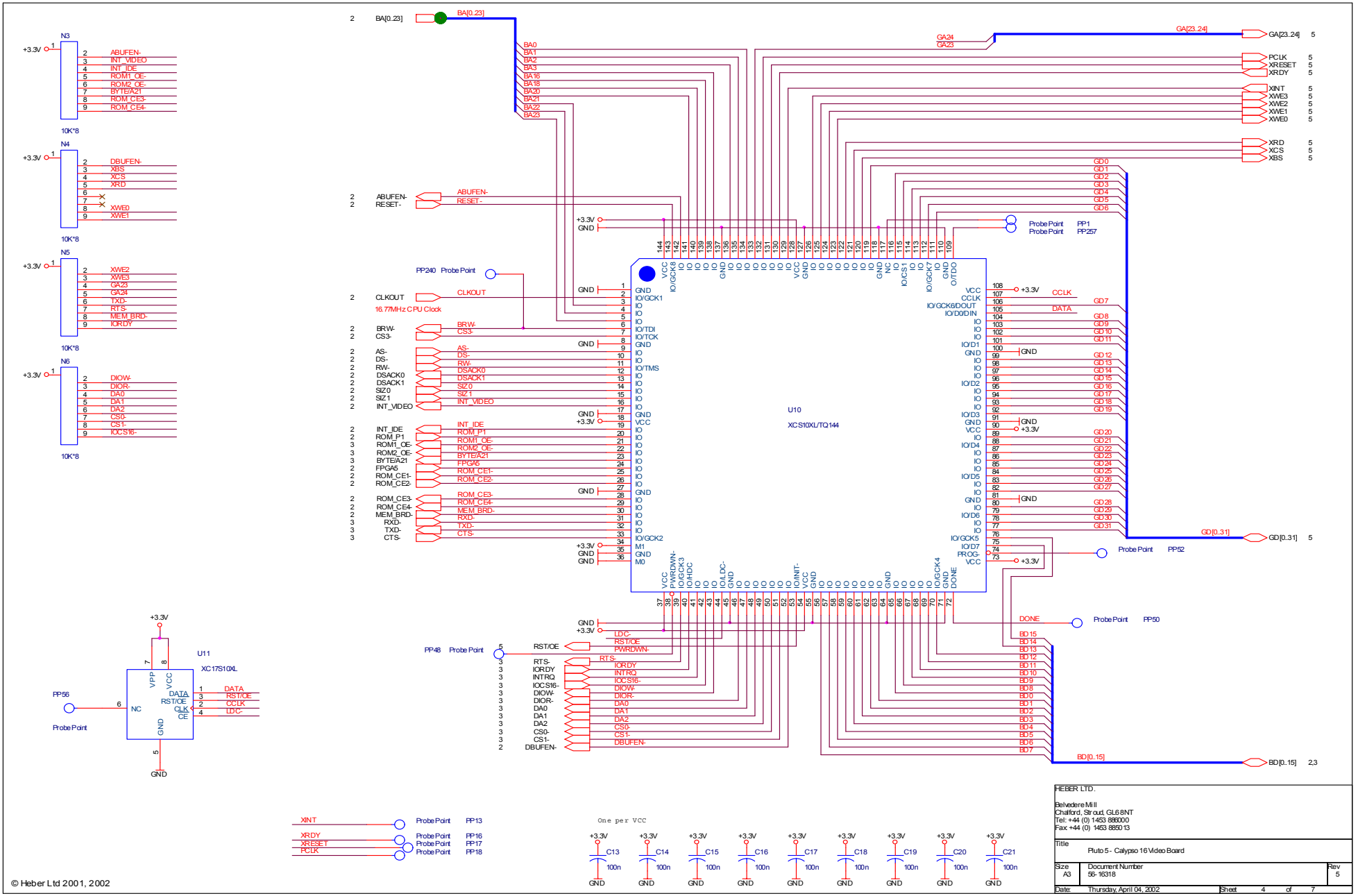


Figure 5 - Calypso 16, Schematic Sheet 5

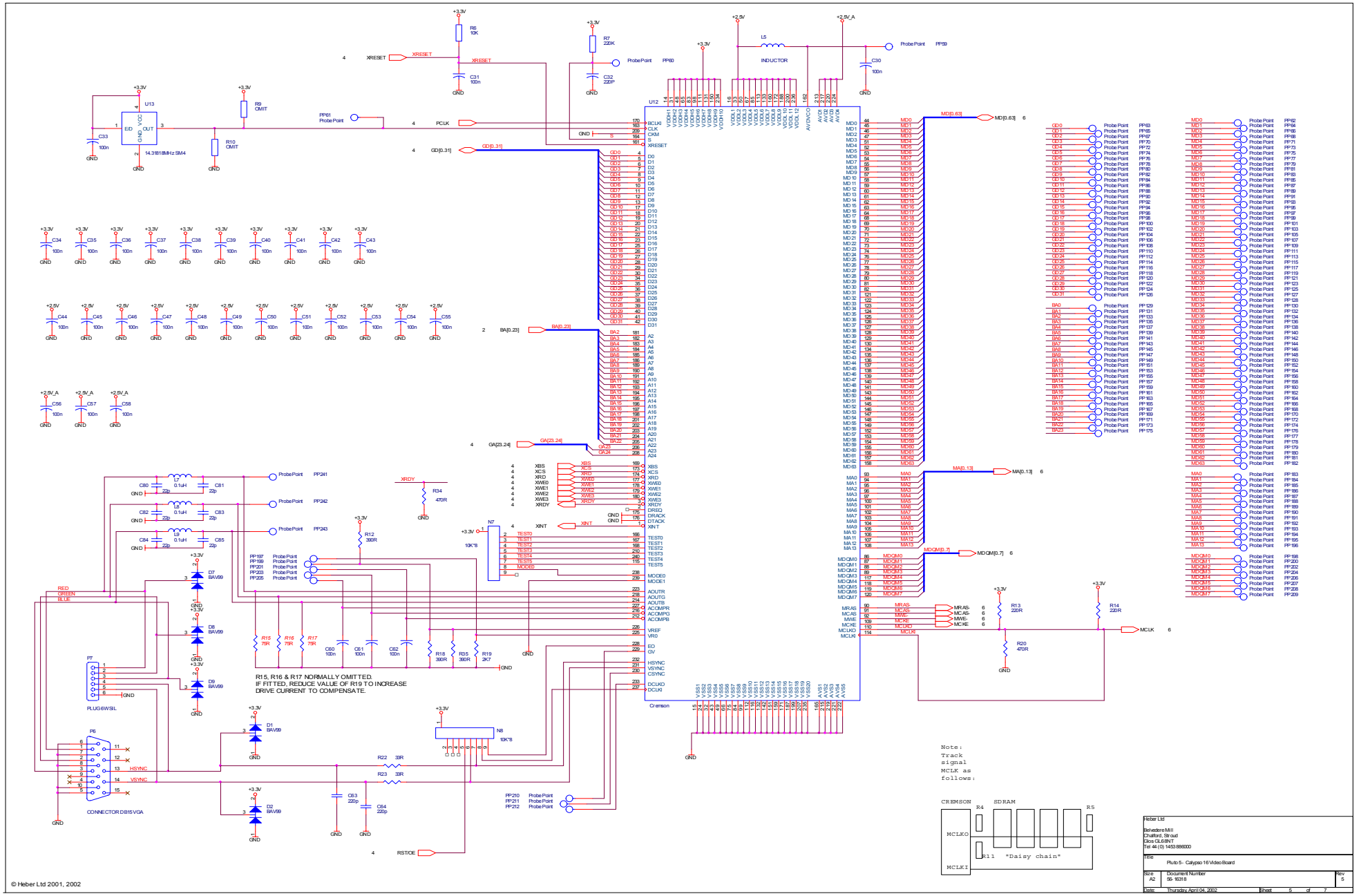


Figure 6 - Calypso 16, Schematic Sheet 6

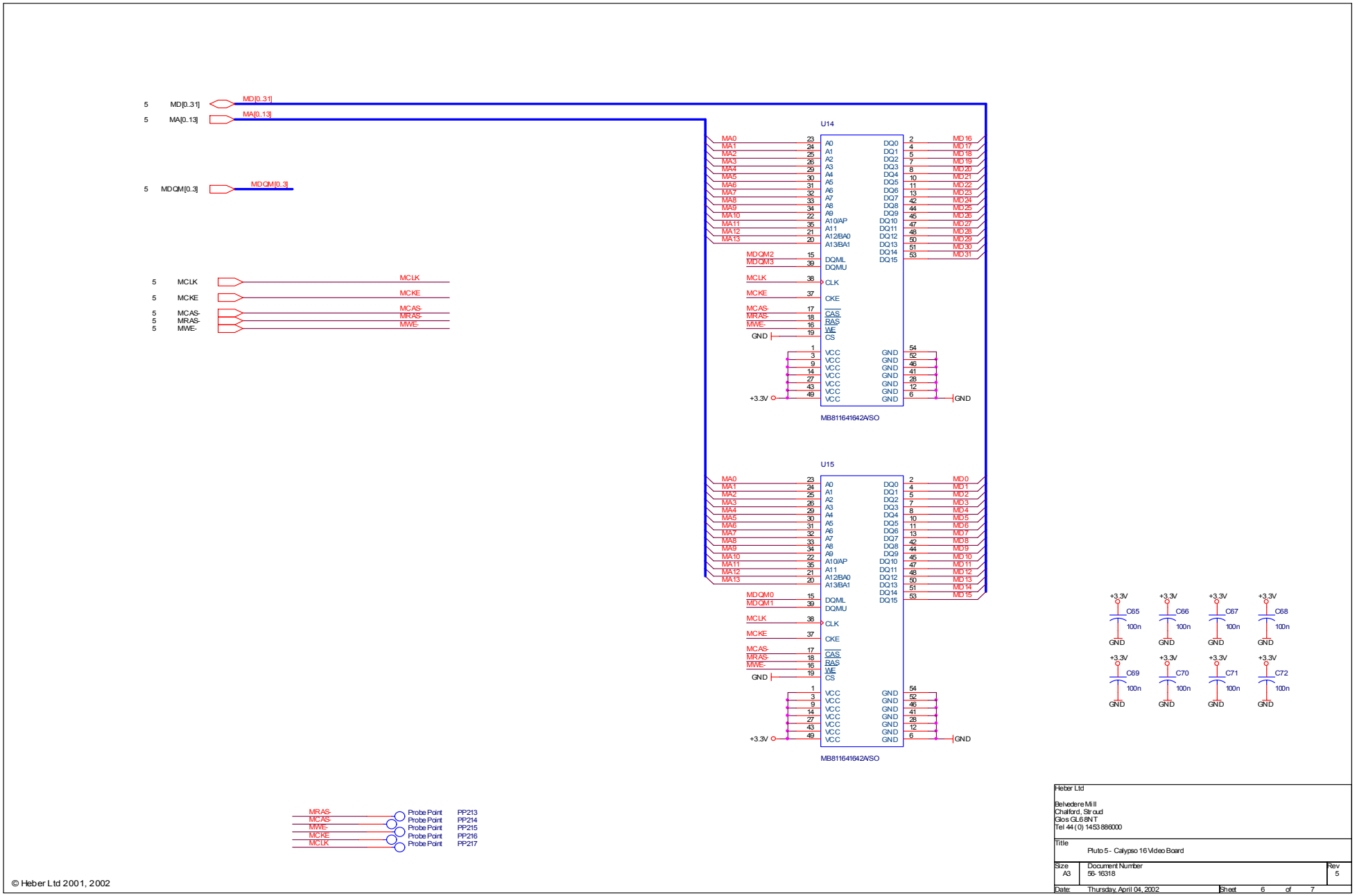


Figure 7 - Calypso 16, Schematic Sheet 7

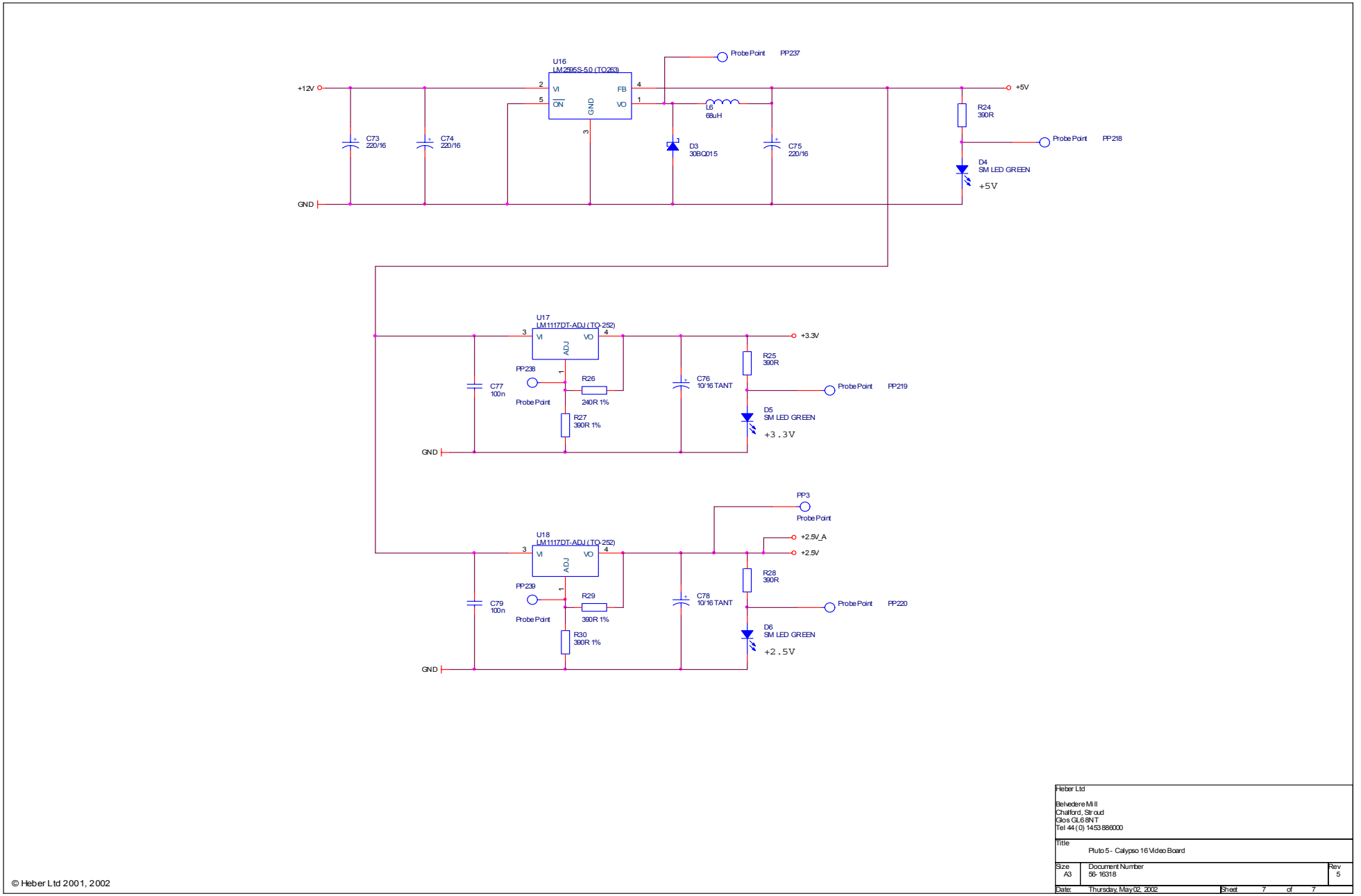


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Figure 8 - Calypso 16, Photograph